PATENT
Attorney Docket No. 85773-40D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: John Gordon Hogeboom

Serial No.: Filed:

Examiner: Group Art Unit:

For: **PARALLEL DATA BUS INTEGRATED CLOCKING AND CONTROL**

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents

Washington, D.C. 20231

Sir/Madam:

Kindly amend this patent application as follows and examine the application in view of the amendments and remarks provided.

I. AMENDMENTS

In the Specification

Please replace the paragraph beginning at page 1, line 4, with the following rewritten paragraph:

-- This is a divisional of Application no. 09/002,113 filed December 31, 1997, which is a continuation-in-part of Application no. 08/997,777 filed December 24, 1997. --

Please insert the following new paragraph at page 5, between lines 9 and 10:

-- FIG. 4 illustrates a block diagram of the high speed bus structure, in accordance with an example of implementation of the

present invention. --

Please replace the paragraph beginning at page 5, line 17, with the following rewritten paragraph:

-- In order to allow maximum data rate, optimum matching between clock and data, and avoidance of special wiring or interfaces, the clock signal in the present high speed clock-with-data communication scheme consists of high and low periods in integer units of bit time. This implies that the clock frequency f_c must be the data bit frequency f_d divided by an integer of two or more, i.e. $f_c = f_d / n$ $(n \geq 2)$, which in turn requires that some means such as a delay-locked loop (DLL) or a phase-locked loop (PLL) must be used to generate a full bit-rate clock or multiple phases separated by one bit time. The same means are also generally useful for producing the fractional-width time phases or delays needed to adjust the previously mentioned clock vs. data phasing. --

In the Claims

Kindly cancel claims 1-14 from the application.

Kindly add the following new claims:

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Claim 16. (new) A data communication system, comprising:

a) a first input for receiving data, said data being characterized by a bit time;

b) a second input for receiving data control information;

c) an encoder unit coupled to said first and second inputs, said encoder unit operative to:

i) generate clock information;

ii) process said clock information and said data control information for generating a clock and control signal, said clock and control signal having high and low times in units equal to one said bit time;

d) at least one data channel; and

e) a clocking and control channel, said encoder unit operative to transmit said data over said at least one data channel and to transmit said clock and control signal over said clocking and control channel.

Claim 17. (new) A data communication system as defined in claim 16, wherein said clock and control signal is characterized by first and second edges, said first edge having fixed phase and said second edge being phase-modulated.

Claim 18. (new) A data communication system as defined in claim 16, wherein said clocking and control channel is characterized by a clock rate and said at least one data channel carries data multiplexed at a multiplexing cycle rate, said clock rate being substantially equal to said multiplexing cycle rate.

Claim 19. (new) A data communication system as defined in claim 17, wherein said first edge carries bit timing information for clock synchronization.

Claim 20. (new) A data communication system as defined in claim 17, wherein said second edge carries at least data control information.

Claim 21. (new) A data communication system as defined in claim 17, wherein said second edge carries at least data

framing data.

Claim 22. (new) A data communication system as defined in claim 17, wherein said second edge carries data control information and framing data.

Claim 23. (new) A data communication system as defined in claim 16, wherein said data communication system further comprises:

a) a decoder unit for receiving data and the clock and control signal over said data channel and said clocking and control channel, respectively, said decoder unit operative to:

i) extract from said clock and control signal said clock information and said data control information;

ii) process said data on a basis of said clock information and said data control information for generating a data signal;

b) an output for releasing said data signal to a data processing device.

Claim 24. (new) A data communication system as defined in claim 23, wherein said data channel is selected from the group consisting of a cable, an optical fiber and an air interface.

Claim 25. (new) A data communication system as defined in claim 23, wherein said clocking and control channel is selected from the group consisting of a cable, an optical fiber and an air interface.

Claim 26. (new) An encoder for use in a data communication system, said encoder connected to at least one data channel and a clocking and control channel, said

encoder comprising:

a) a first input for receiving data, said data being characterized by a bit time;

b) a second input for receiving data control information;

c) a processing unit operative to:

i) generate clock information;

ii) process said clock information and said data control information for generating a clock and control signal, said clock and control signal having high and low times in units equal to one said bit time;

d) a first output for transmitting said data over the at least one data channel;

e) a second output for transmitting said clock and control signal over the clocking and control channel.

Claim 27. (new) A decoder for use in a data communication system, said decoder connected to at least one data channel and a clocking and control channel, said decoder comprising:

a) a first input for receiving data over the at least one data channel, said data being characterized by a bit time;

b) a second input for receiving a clock and control signal over the clocking and control channel, said clock and control signal said clock and control signal having high and low times in units equal to one said bit time;

c) a processing unit operative to:

i) extract from said clock and control signal clock information and data control information;

ii) process said data on a basis of said clock

information and said data control information for generating a data signal;

d) an output for releasing said data signal to a data processing device.

Claim 28. (new) A data communication system, comprising:

a) first input means for receiving data, said data being characterized by a bit time;

b) second input means for receiving data control information;

c) encoder means coupled to said first and second input means, said encoder means operative to:

i) generate clock information;

ii) process said clock information and said data control information for generating a clock and control signal, said clock and control signal having high and low times in units equal to one said bit time;

d) at least one data channel; and

e) a clocking and control channel, said encoder means operative to transmit said data over said at least one data channel and to transmit said clock and control signal over said clocking and control channel.

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ATTATCHED HERETO IS A MARKED UP VERSION OF THE AMENDMENTS MADE TO THE SPECIFICATION BY THE PRESENT AMENDMENT. THE ATTACHED PAGE IS CAPTIONED "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

II. SUMMARY OF AMENDMENTS

Amendments have been made to the specification in order to clarify any ambiguity and to conform to standard format requirements. The Applicant respectfully submits that no new matter has been added.

Claims 1-14 have been cancelled from the application.

New claims 16 to 28 have been added to the application.

III. REMARKS

The present application is a divisional of U.S. patent application serial no. 09/002,113, filed December 31, 1997. Patent application serial no. 09/002,113 was under the responsibility of Examiner F. Duong and was assigned Group Art Unit 2664.

During prosecution of patent application serial no. 09/002,113, an amendment was filed July 25, 2000 in response to an Office Action mailed April 25, 2000, in which new claims 15-28 were added to the application. A Final Office Action was mailed on September 29, 2000 in which the Examiner found that restriction to one of the following inventions was required under 35 U.S.C. 121:

I. Original claims 1-14 and newly added claim 15, drawn to system processing synchronization, classified in class 370, subclass 503.

II. Newly added claims 16-28, drawn to encoder and decoder for generating and processing synchronization signals with unique length,

classified in class 375, subclass 364.

Accordingly, in a Response filed on November 29, 2000, the Applicant acknowledged the above restriction requirement and elected claims 1-15 directed to invention I, for prosecution on the merits in application 09/002,113. At that time, the Applicant reserved the right to file a divisional application directed to withdrawn claims 16-28, prior to issuance to patent of application 09/002,113.

IV. CONCLUSION

Allowance of claims 16 to 28 at an early date is solicited.

If the claims of the application are not believed to be in full condition for allowance, for any reason, the Applicant respectfully requests the constructive assistance and suggestions of the Examiner in drafting one or more acceptable claims or in making constructive suggestions so that the application can be placed in allowable condition as soon as possible and without the need for further proceedings.

Respectfully submitted,

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Date: June 7, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

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